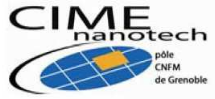


Microsystem & transistor fabrication on a silicon substrate

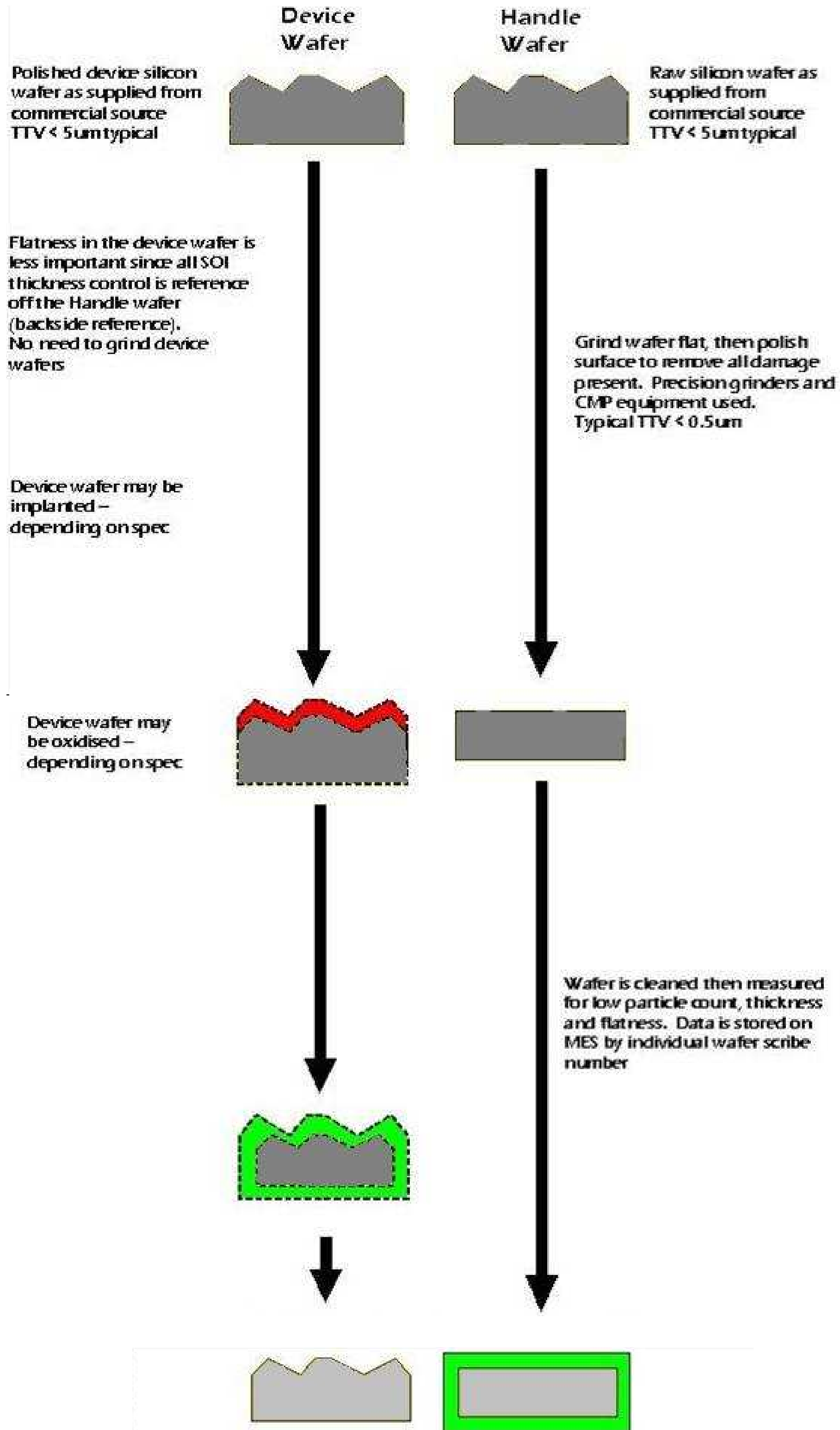
CIME nanotech pôle CNFM de Grenoble

T NMOS grille Si poly + MICROSYSTEMES: masques MEMS

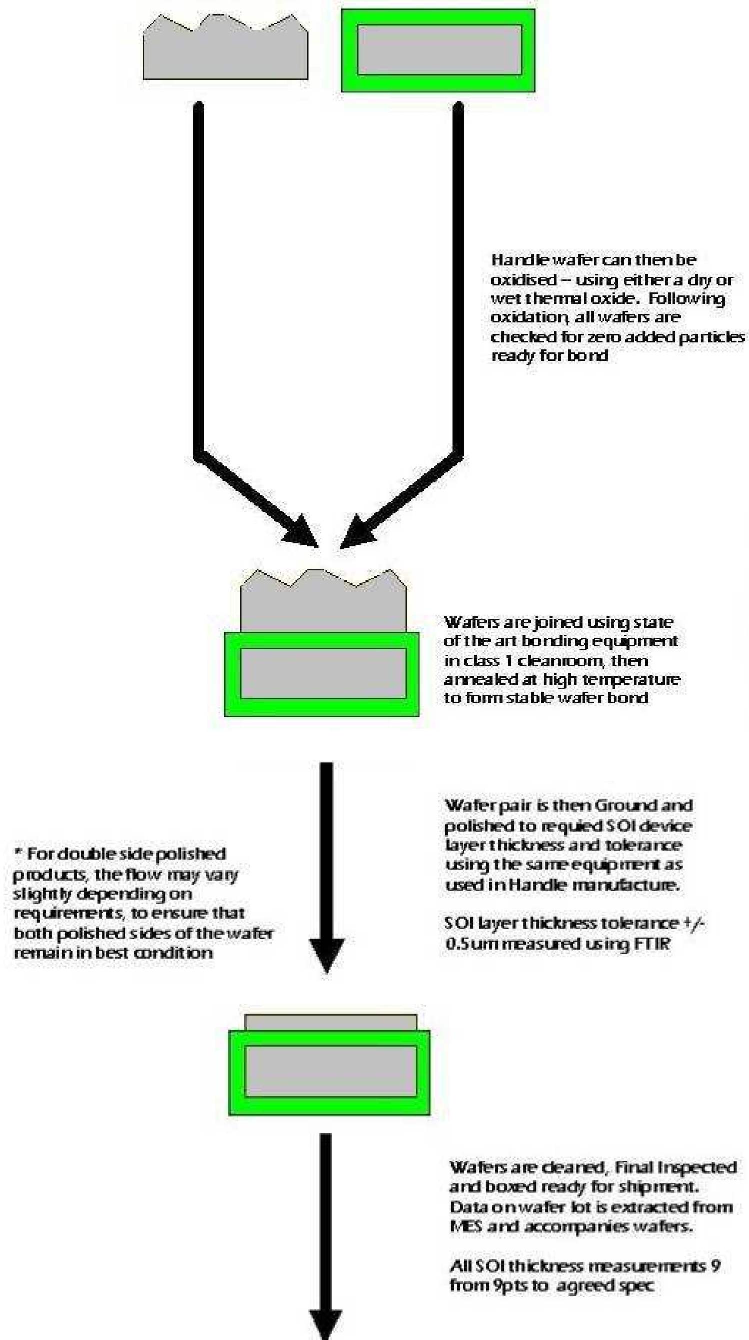
Organisation MEMS actuelle en 16h
Étapes sous-traitées au CIME pour préparation de plaques: *(1) nettoyage* *(1bis) désoxydation FAR des plaques SOI* *(2) oxydation thermique humide* *(3) photolithographie* *(4) ouverture des zones actives*
Étapes sous-traitées au LAAS: *(5) Nettoyage* *(6) oxydation thermique sèche* *(7) dépôt Si poly*
S1: photolithographie Si poly - RIE
S2: implantation **Gravure oxyde en face arrière du wafer SOI avec protection de la face avant du wafer par de la résine** **Retrait résine + nettoyage** **Recuit d'implantation**
Étape sous-traitées: désoxydation et mise sous vide pour dépôt alu
S3: dépôt alu – photolithograhie et gravure alu
S4: photolithographie résine épaisse FAR - DRIE

Fourniture par groupe de 4 étudiants:
- une plaque 4 pouces polies double face
- une plaque SOI

SOI wafers



SOI wafers



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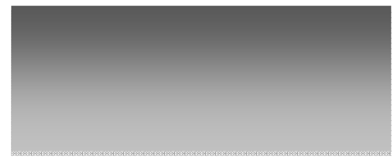
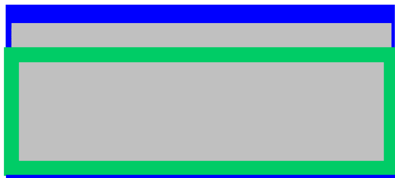
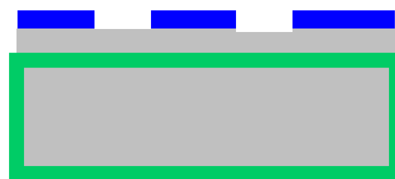
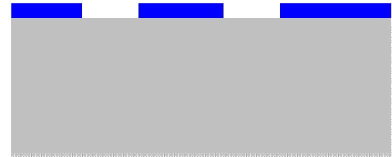
wafer SOI		wafer Si
	• Cleaning HF 5% H_2O_2/H_2SO_4 HF 5%	
	• Thick oxide growth (300 nm)	
	• Photolithography via opening windows mask and wet etching	

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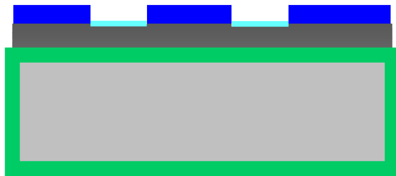
wafer SOI

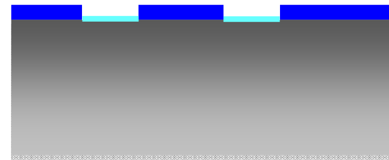
MEMS pressure sensor *MOS transistor*

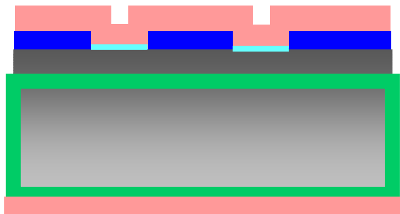


- Thin oxide growth (450 Å, dry oxidation at 1050° C)

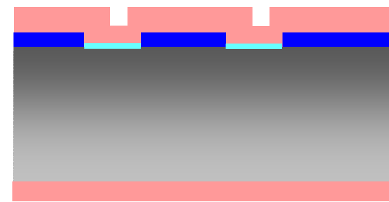
wafer Si

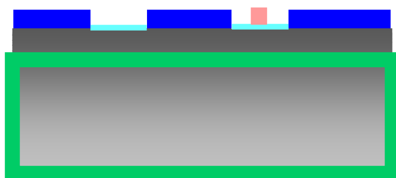
MEMS pressure sensor *MOS transistor*



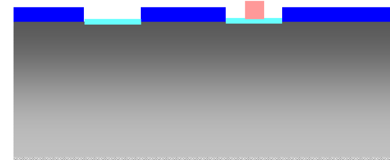


- Poly-silicon CVD (250 nm)





- Poly silicon photo lithography (mask Poly) + RIE on both sides



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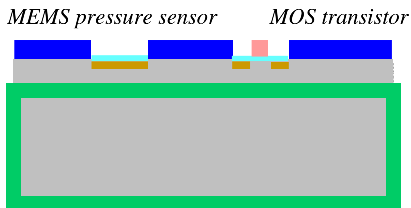
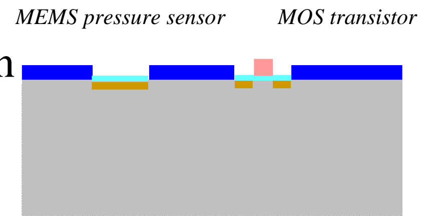
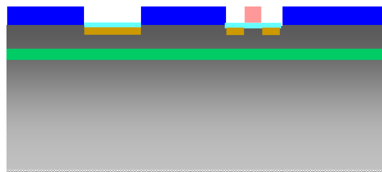
wafer SOI

wafer Si

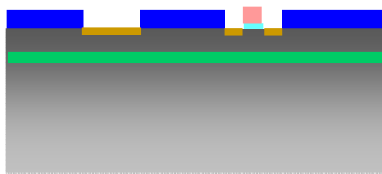


- Ion implantation $3.10^{E}15$ at/cm² @ 70keV



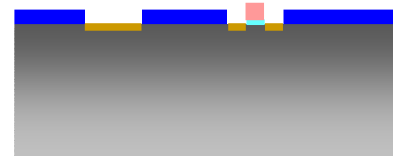


- for SOI wafer : Resist Spin coating + back-side Oxide Etching + stripping



- Annealing (950° C, 20 min, nitrogen atmosphere)

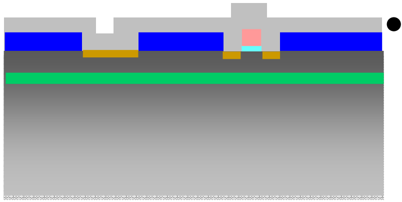
- Thin oxide etching



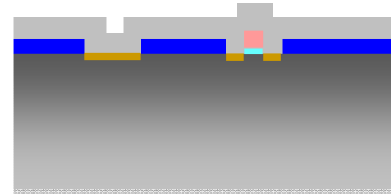
CIME nanotech
pôle CNFM de Grenoble

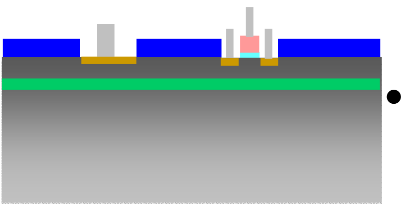
wafer SOI | wafer Si

MEMS pressure sensor *MOS transistor* | *MEMS pressure sensor* *MOS transistor*

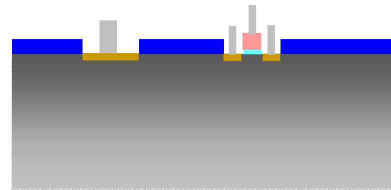


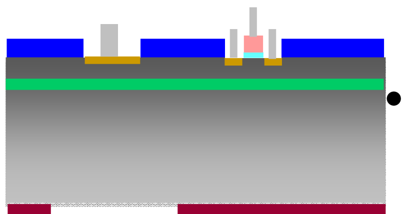
- Aluminum sputtering



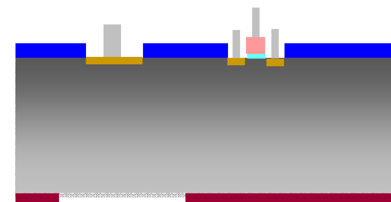


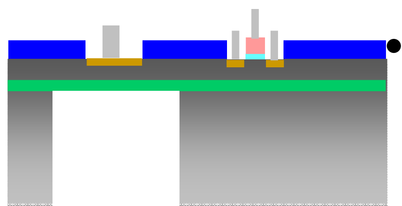
- Aluminum photolithography + wet etch



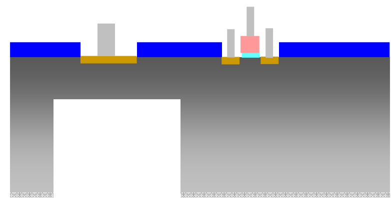


- Back side photolithography





- DRIE on SOI wafer + photoresist stripping



MEMS pressure sensor *MOS transistor*